UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,621	06/26/2003	Robert J. Mears	62604	4467

27975 7590 11/23/2005

ALLEN, DYER, DOPPELT, MILBRATH & GILCHRIST P.A.
1401 CITRUS CENTER 255 SOUTH ORANGE AVENUE
P.O. BOX 3791
ORLANDO, FL 32802-3791

EXAMINER	
TSAI, H JEY	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 11/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/603,621	MEARS ET AL.	
	Examiner	Art Unit	
	H.Jey Tsai	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/3/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 8-11 are rejected under 35 U.S.C. § 102(b) as being anticipated by Tsu 5,216,262, cited by applicant.

Tsu discloses a method of forming a semiconductor structure comprising the steps of:

forming first, second, third and fourth atomic layers of silicon (monoatomic n layers of $(Si/SiO_2)_n$), fig. 2 and col. 3, lines 35-41,

forming a fifth atomic layer of oxygen (SiO_2) on the fourth atomic layer of silicon on a substrate,

forming sixth, seventh, eighth, and ninth atomic layers of silicon (monoatomic n layers of $(Si/SiO_2)_n$), on the fifth atomic layer of oxygen (SiO_2), fig. 2, 4,

forming a tenth atomic layer of oxygen (SiO_2) on said ninth atomic layer of silicon (monoatomic n layers of $(Si/SiO_2)_n$), col. 5, lines 14-50,

forming a channel region ($(Si)_n$, (MOSFET inherently includes channel region, col. 4, lines 46-47),

forming a first plurality of atomic layers $(Si)_n$ of a semiconductor on a substrate (Si), fig. 2, 4,

forming a first atomic layer of a non-semiconductor $(SiO_2)_n$ on the plurality of atomic layers of a semiconductor $(Si)_n$,

forming a second plurality of atomic layers of a semiconductor $(Si)_n$ on the atomic layer of the non-semiconductor $(SiO_2)_n$,

forming a second atomic layer of a non-semiconductor $(SiO_2)_n$ on said second plurality of atomic layers of a semiconductor $(Si)_n$,

wherein the high-conductivity region is a channel region (MOSFET inherently includes channel region).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsu 5,216,262, cited by applicant in view of Nakzato et al. EP 0 843 361, both are cited by applicant.

The reference(s) teach the features :

Tsu discloses a method of forming a semiconductor structure comprising the steps of:

forming first, second, third and fourth atomic layers of silicon (monoatomic n layers of $(Si/SiO_2)_n$), fig. 2 and col. 3, lines 35-41,

forming a fifth atomic layer of oxygen (SiO_2) on the fourth atomic layer of silicon on a substrate,

forming sixth, seventh, eighth, and ninth atomic layers of silicon (monoatomic n layers of $(Si/SiO_2)_n$), on the fifth atomic layer of oxygen (SiO_2), fig. 2, 4,

forming a tenth atomic layer of oxygen (SiO_2) on said ninth atomic layer of silicon (monoatomic n layers of $(Si/SiO_2)_n$), col. 5, lines 14-50,

forming a channel region ($(Si)_n$, (MOSFET inherently includes channel region, col. 4, lines 46-47),:

forming a first plurality of atomic layers $(Si)_n$ of a semiconductor on a substrate (Si), fig. 2, 4,

forming a first atomic layer of a non-semiconductor $(SiO_2)_n$ on the plurality of atomic layers of a semiconductor $(Si)_n$,

forming a second plurality of atomic layers of a semiconductor $(Si)_n$ on the atomic layer of the non-semiconductor $(SiO_2)_n$,

forming a second atomic layer of a non-semiconductor $(SiO_2)_n$ on said second plurality of atomic layers of a semiconductor $(Si)_n$,

wherein the high-conductivity region is a channel region (MOSFET inherently includes channel region).

The difference between the reference(s) and the claims are as follows: Tsu teaches forming n layers of monoatomic semiconductor and non-semiconductor layers for a MOSFET device but does not show the source/drain region of N-type and substrate of p-type. However, Nakzato et al. teaches at col. 12, lines 15-50 and fig. 5, a n-type source/drain regions 5, 6 and a p-type substrate 3.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have recognized that a MOSFET includes a n-type source/drain regions and a channel region as suggested by Nakazato et al. because source/drain region and channel region formed in the substrate would complete a MOSFET device.

Any inquiry of a general nature or clerical matters or relating to the status of this application or proceeding should be directed to the customer service whose telephone number is (703) 308-4357.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to H. Jey Tsai whose telephone number is (571) 272-1684. The examiner can normally be reached on from 7:00 Am to 4:00 Pm., Monday thru Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873.

The fax phone number for this Group is 571-273-8300.

hjt

11/19/2005

H. Jey Tsai
Primary Examiner
Patent Examining Group 2800